APPLICATION FOR

UNITED STATES PATENT

in the name of

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for

INTEGRATED SEMICONDUCTOR MEMORY WITH A SELECTION TRANSISTOR FORMED AT A WEB

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CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 USC §119 to German Application No. 10256973.8, filed on December 5, 2002, and titled "Integrated Semiconductor Memory With A Selection Transistor Formed at a Web," the entire contents of which are hereby incorporated by reference.

FIELD OF THE INVENTION

The invention relates to an integrated semiconductor memory, and more particularly, an integrated semiconductor memory with a memory cell having a storage capacitor and a selection transistor.

BACKGROUND

Integrated semiconductor memories have a memory cell array with a multiplicity of memory cells for storing digital information and also a logic region for driving the memory cell array and for operating the semiconductor memory. Storage is effected in storage capacitors, which are driven via a selection transistor situated at the crossover point between a word line, which electrically opens or closes the transistor, and a bit line. Further transistors are arranged in the logic region, and are constructed differently and dimensioned differently than selection

transistors of memory cells. In particular, the minimizing space by the memory region on the wafer area and the desired analog switching behavior of transistors of an analog logic region yield different selection criteria for transfer design for the two regions.

One design of the selection transistor in the memory region is the surrounding gate transistor. Webs made of substrate material formed by a perpendicular etching are used as a basic structure for the formation of the transistor. In this case, the patterned, usually elongate, web is covered with a gate dielectric and surrounded from all sides, except for the top side, with a peripheral gate electrode formed by a spacer technique. A trench capacitor is arranged at one end of the web. A first, lower source/drain region is formed by outdiffusion from the inner capacitor electrode of the trench capacitor. On the top side of the web, a second, upper source/drain region is implanted so that a vertical selection transistor is produced at one lateral end of the web at which the trench capacitor is situated. Alternatively, the vertical selection transistors can be formed in the interior of a capacitor trench above the storage capacitor.

Furthermore, there are semiconductor memories with planar selection transistors in the memory cell array, which are arranged laterally with respect to the connected storage capacitors. These selection transistors do not have a web made of substrate material.

These designs of selection transistors are usually realized in circuitry terms by field-effect transistors, in particular, MOSFETs (metal oxide semiconductor field effect transistors), in which, between two source/drain regions below a gate dielectric, an electrically conductive channel is formed by inversion of doped substrate material. The inversion channel has a channel length between the source and the drain, and a channel width, which corresponds to the optical resolution limit used.

In view of decreasing operating voltages and decreasing lateral dimensions of the memory cells with limited current density, the write and read speed cannot be increased sufficiently to the desired extent.

Moreover, leakage currents, which flow *inter alia* via the electrical connection between storage capacitor and selection transistor, cause a premature discharge of the storage capacitor which, in the case of volatile semiconductor memories, shortens the refresh period and drives up the current consumption of the memory.

SUMMARY

An integrated semiconductor memory can be operated with a higher current for writing in and/or reading out information and which can be less susceptible to leakage currents. Generally, an integrated semiconductor including a web arranged on an insulation layer, a first source/drain region arranged on the insulation layer at one lateral end of the web, and a second source/drain region is arranged on the insulation layer at another lateral end of the web. Also, the two longitudinal sides of the web and a top side of the web can be covered with a layer sequence comprising a gate dielectric and a gate electrode.

A memory cell in a memory cell array can include a transistor in which the transistor channel's current flow direction can run parallel to the insulation layer. The transistor can be provided at a web made of substrate material. The current flow direction can also parallel the longitudinal direction of the web. Both longitudinal sides and the top side of the web can be covered by a gate dielectric and a gate electrode can be arranged above the gate dielectric. This can result in a significantly larger channel width than in conventional selection transistors, since twice the web height (in each case at the left-hand and right-hand longitudinal side of the web)

and the web width together produce the channel width. Consequently, by large web heights, without enlarging the basic area of the memory cell, it is possible to achieve high channel widths, i.e., high currents for storing and reading out information, as a result of which the write and read speed of the semiconductor memory can increase.

At the same time, the potential leakage currents in the off state of the transistor, i.e., when no channel is formed, can be reduced, since the transistor and its conductive connection to the storage capacitor can be isolated from the semiconductor substrate by the buried insulation layer. As a result, a more reliable insulation can be achieved than when lower source/drain contacts are formed by outdiffusion of the surrounding gate transistors, in which the conductive connection between selection transistor and storage capacitor is formed by a dopant diffusion extending into the semiconductor material.

In the semiconductor memory, the selection transistor formed at the web can be situated above the buried insulation layer. The insulation layer can be an oxide layer and can be insulated from adjacent memory cells by the buried insulation layer. Shallow trench isolations and also collar regions can thus be obviated.

Consequently, conflicting design requirements of the transistor can be better reconciled than a conventional semiconductor memory.

The storage capacitor can be a trench capacitor whose inner capacitor electrode can be isolated from an outer capacitor electrode below the buried insulation layer by a capacitor dielectric, which extends as far as the bottom of the storage capacitor. In conventional trench capacitors, a collar region is provided in an upper region to prevent the formation of parasitic transistors, which leads to constriction of the inner capacitor electrode. As a result the latter is isolated from the outer capacitor electrode, formed by the semiconductor material of the

substrate, in the upper region not only by the capacitor dielectric but also by the collar region, which does not extend as far as the bottom of the capacitor. The storage capacitor can only be produced below a certain depth corresponding to the height of the collar region.

In the case without a collar region, by contrast, the storage capacitor can be formed as far as the buried insulation layer arranged directly below the web, as a result of which its capacitance rises.

The inner capacitor electrode of the storage capacitor can extend as far as the underside of the buried insulation layer and can be connected by a surface contact to the first source/drain region of the selection transistor. The surface contact can be situated at the level of and above the buried insulation layer, and can be electrically insulated by the latter from the substrate material situated at a deeper level. Consequently, leakage currents between the storage capacitor and the selection transistor rarely occur in this region.

The top side of the surface contact can be arranged below the level of the top side of the web and cab be electrically insulated from a word line passing the storage capacitor by an insulating upper filling structure. This word line (passing word line) can be formed at the same level as the word line, which can be connected to the selection transistor and can cover the top side of the web. The passing word line running at the same level can be insulated from the top side of the upwardly shortened surface contact by the upper filling structure.

The semiconductor substrate can be doped below the buried insulation layer. The use of an SOI substrate (silicon on insulator) in conjunction with the selection transistor designs can enable good insulation of the current path between a selection transistor and the storage capacitor connected thereto from other adjacent memory cells and also from the semiconductor substrate situated at a deeper level.

The second source/drain region can have, in the longitudinal direction of the web, the same dimension, i.e., the same width, as the underside of a spacer of a word line covering the web. The second source/drain region can be connected to a bit line contact on the side remote from the web. Consequently, one of the source/drain regions can be with the aid of the word line spacer. That side area of the source/drain region which is remote from the web may be connected by a bit line contact to a bit line running above the web and above the word line.

Accordingly, a bit line can be arranged above the web, can run parallel to the longitudinal direction of the web, and can be connected to the second source/drain region. By this bit line, webs, which can be strung together in their longitudinal direction and can be interrupted by capacitor trenches, may be contact-connected at a respective end via the bit line contact. In the direction of the word lines adjacent to the webs and at a level below the bit lines, provided that no word lines run there, the memory cell array can be filled with an insulating material, for example, an oxide or nitride.

A word line can run perpendicular to the longitudinal direction of the web, and can cover the gate dielectric on both longitudinal sides and on the top side of the web. The gate electrode that is formed by the word line and is isolated from the semiconductor material of the web only by the gate oxide layer at both side walls of the web which run in the longitudinal direction, leads to a channel width which is only limited by the web height. The channel width can thus be chosen to be larger than the structure width (critical dimension), i.e., the optical resolution limit used in the lithographic patterning. The web may be patterned in a manner narrower than the optical resolution limit. For example, it may be narrower than the bit line running above it. The channel width is not appreciably impaired thereby, since essentially the web height contributes to the channel width.

The semiconductor memory can have a multiplicity of memory cells of the semiconductor memory with selection transistors formed at webs, a bit line contact being arranged only at every second crossover point between a bit line and a word line and a word line passing above or below a storage capacitor at the remaining crossover points. The selection transistors formed at the webs can thus be arranged relative to the direction of the word lines and bit lines in a diagonal grid of selection transistors that are the most closely adjacent to one another.

The integrated semiconductor memory can be a dynamic read-write memory, in particular, a DRAM (dynamic random access memory).

The details of one or more embodiments are set forth in the accompanying drawings and the description below. Other features will be apparent from the description and drawings and from the claims.

BRIEF DESCRIPTION OF FIGURES

FIG. 1 is a cross-sectional view of a semiconductor memory according to the invention,

FIG. 2 is another cross-sectional view, taken along the line C-C in FIG. 1, and

FIG. 3 is a plan view of the semiconductor memory of FIG. 1.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

FIG. 1 shows an integrated semiconductor memory 10 with an SOI substrate 20. The buried insulation layer 11 can be arranged directly below the selection transistors 3 of the memory cells 1. The selection transistors can be formed at webs 4. The buried insulation layer,

preferably oxide layer 11, can have openings in which a trench capacitor 2 can be incorporated into the substrate 20 and can be connected to a first source/drain region 5 of the selection transistor 3 by a contact arranged in the opening, a surface contact 19. The first source/drain region 5 can be situated at a first end A of the web 4 running in the longitudinal direction x, and the second source/drain region 6 can be arranged at the other lateral end B of the web. The web can extend between the ends A, B with its main extending direction x, which can coincide with the current flow direction I of the transistor channel, and can be surrounded from above and also on its side walls above and below the plane of the drawing by a gate oxide 9 and a gate layer sequence 16.

In contrast to conventional storage capacitors, the storage capacitor 2 does not have a collar region. Instead, the inner capacitor electrode 12 can be isolated from an outer capacitor electrode 18, in a depth directly below the insulation layer 11, only by a capacitor dielectric 13, which can extend as far as the bottom 26 of the storage capacitor.

FIG. 2 is a cross-sectional view, taken along the line C-C of FIG. 1, i.e., perpendicular to the plane of the drawing of FIG. 1. In FIG. 2, the transistor channel runs perpendicularly to the plane of the drawing through the web, along the two side areas 14 and along the top side 15. There, the gate layer sequence 16, can be composed, for example, of a lower gate layer 7, for instance, made of polysilicon, and an upper gate layer, which may contain tungsten, can be isolated from the channel region of the web 4 only by the gate oxide 9 or some other dielectric.

The dimensions in FIG. 2 are not illustrated to scale. The web height can be greater than the optical resolution limit used in the lithographic exposure during the fabrication of the semiconductor memory. In particular, the web height and thus the height of the side areas 14 may be greater than the distance between the bit lines 17, thus resulting in a larger channel width

than in the case of a conventional selection transistor. In FIG. 2, the oxide layer 11 can be arranged below the web and the bulk material of the substrate 20, which can be doped, in particular, heavily n-doped, can be arranged below the oxide layer. Alternatively, the doping of the web 4 may be adapted to the desired electrical properties of the selection transistor. In particular, the semiconductor material of the web 4 may be doped with a different doping type, a different dopant and/or a different dopant concentration than the semiconductor material 20 below the buried oxide layer 11. In FIG. 2, the bit line 17 can be insulated from the word line 16 by an oxide layer 22 or a different dielectric.

The web 4, illustrated in cross section perpendicular to the current direction in FIG. 2, can run from right to left between the first and second source/drain regions 5, 6 in FIG. 1. The surface contact 19 can have a top side arranged at a deeper level than the top side 15 of the web 4 and may therefore readily be covered by an insulating filling structure 30, for example, an oxide, before a passing word line 16a can be deposited above the capacitor trench. An insulation layer 22 can be deposited in order to insulate the word lines from the bit lines.

The storage capacitor 2 can have as outer capacitor electrode, either an electrode (buried plate) which can be arranged below the buried insulation layer 11 and can be arranged in the bulk material, or can include the doped, for example, heavily n-doped, substrate material of the semiconductor substrate 20. The inner capacitor electrode 12 can be isolated from the substrate 20 by a capacitor dielectric 13, which may also be a layer sequence, in a topmost region below the insulation layer 11, where a collar region can be provided. The electrical connection between the inner capacitor electrode 12 and the first source/drain region 5 of the selection transistor 3 is produced by a surface contact 19.

The surface contact 19 and the selection transistor 3 can be insulated from the semiconductor material of the semiconductor substrate 20 by the buried insulation layer 11, so that leakage currents can be smaller in this region than in conventional semiconductor memories.

FIG. 3 shows, in plan view, an arrangement of seven storage capacitors 2, which are connected toward the right-hand side to a respective selection transistor 3 formed in each case at a web 4. The storage capacitors 2 can be arranged below the buried insulation layer 11, whereas the selection transistors 3 can be arranged above the buried insulation layer 11. The word lines 16 can cross the longitudinal direction x of the webs 4 and can cover both longitudinal sides and the top side of the webs. As a result, a large channel width can be obtained. By using narrow webs which may be configured narrower in direction y, with the aid of spacers, than the distance between the bit lines 17, charge carriers in the semiconductor material of the web can be depicted, so that an ideal on/off current characteristic of the selection transistor 3 can be achieved. The subthreshold transconductance of such a transistor can be higher than a conventional transistor. A higher current can be achieved with a significantly reduced voltage at the gate. This affords advantages over conventional memory types, for instance, a higher current consumption and a smaller area taken by the circuits.

In FIG. 3, the webs can be arranged in rows along the bit lines 17 running above them. Adjacent webs 4 in direction y of the word lines 16 can be offset with respect to one another in the x direction, so that such adjacent memory cells, which can be driven by two different word lines 16, can be simultaneously connected by two different bit lines 17.

During fabrication of the semiconductor memory, an SOI substrate, which may be doped below its oxide layer 11, can be covered with a layer sequence for etching a mask for the

patterning of capacitor trenches. Such a layer sequence may, for instance, include an oxide, a nitride, a borosilicate glass, or a polysilicon.

The photolithographic etching of the capacitor trenches can be followed by the deposition of the capacitor dielectric (for instance, a nitride, oxide, an aluminum oxide, etc.) and, on the latter, the inner capacitor electrode can be made, for example, of heavily n-doped polysilicon. The material of the inner capacitor electrode can be etched back at most as far as the lower edge of the buried insulation layer 11 of the semiconductor substrate 20. The capacitor dielectric 13 can then be removed at the level of the web.

A polysilicon layer can be deposited and subsequently etched back approximately as far as the level of the top side of the web or a little deeper. Half of each surface contact 19 can be removed in the direction of its nearest left-hand web 4. The resulting opening can be filled with an insulating material, for instance, an oxide 30, which can also cover the top side of the surface contact 19.

Afterward, a hard mask for patterning the webs can be patterned lithographically. In order to fabricate particularly fine hard mask structures for patterning the webs, a spacer can be used as mask. As a result, web widths in the y direction can be narrower than the lithographic resolution limit, which can be used for patterning and with which word lines and bit lines can be patterned. After etching of the surroundings of the webs, the etching mask can be removed, doping of the channel region can be introduced by implantation into the semiconductor material of the web, and a gate oxide layer can be grown.

Polysilicon can be deposited as first gate layer 7 onto the gate oxide layer and can be subject to chemical mechanical polishing in order to deposit above it a second gate layer 8 made of tungsten, for example, and a covering layer made of nitride 23, and subsequently to

lithographically pattern the word line layer sequence can be formed. This patterning can include a nitride etching, a resist removal, a tungsten etching, an etching of polysilicon, and side wall oxidation of the word line.

Afterward, a nitride or a different spacer material can be deposited and can be etched back anisotropically, thereby providing spacers 21, 24. Then, the second source/drain regions can be implanted and can be covered by an oxinitride deposition and a deposition of BPSG (borophosphosilicate glass), which can flow thermally. After the BPSG filling has been polished back as far as the top side of the nitride 23 covering the word lines, an undoped oxide can be deposited and can be patterned lithographically in order to fabricate bit line contact holes for making contact with the second source/drain regions 6, an oxide etching, an oxinitride etching and a silicon etching succeeding one another.

Finally, a metal can be deposited for fabricating the bit line contacts and the bit lines themselves. In this way, a selection transistor with a transistor channel having a horizontal current direction can be fabricated at the webs in the memory cell array, which selection transistor, in the on state, can enable a high write and read current to the storage capacitor 2 and, in the off state, can be insulated from the material of the semiconductor substrate 20 by the buried insulation layer 11.

An integrated semiconductor memory fabricated in this way can include storage capacitors 2, which can extend closer to the surface of the semiconductor substrate, and therefore, can have a slightly larger capacitance than conventional storage capacitors. The storage capacitor may likewise be a stacked capacitor. In particular, a capacitor can be arranged above word lines. In this case, there is no electrical connection between the substrate material and the memory cell. A memory cell can have a semiconductor memory with a basic area of

8 F^2, where F corresponds to the optical resolution limit or typical structure width of structures produced lithographically.

While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof. Accordingly, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

List of Reference Symbols

1	Memory cell
2	Storage capacitor
3	Selection transistor
4	Web
5	First source/drain region
6	Second source/drain region
7	Lower gate layer
8	Upper gate layer
9	Gate dielectric
10	Integrated semiconductor memory
11	Buried insulation layer
12	Inner capacitor electrode
13	Capacitor dielectric
14	Longitudinal side of a web
15	Top side of a web
16	Gate electrode
17	Bit line
18	Inner wall of a storage capacitor
19	Surface contact
20	Semiconductor substrate
21	Spacer
22	Oxide layer
23	Nitride layer
24	Further spacer
25	Insulating filling
26	Bottom of the storage capacitor
30	Insulating filling structure
A, B	Lateral web ends
I	Current flow direction of the transistor channel